UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,542	08/13/2001	Hieu Van Tran	2102397-991720	9808

7590 06/04/2003

EDWARD B. WELLER
GRAY,CARY,WARE & FREIDENRICH LLP
1755 EMBARCADERO ROAD
PALO ALTO, CA 94303-3340

EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/929,542	Applicant(s) TRAN ET AL.	
	Examiner son t dinh	Art Unit 2824	

-- Th MAILING DATE of this communication app ars on the cov r sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-82 and 84-108* is/are pending in the application.

4a) Of the above claim(s) *84-108* is/are withdrawn from consideration.

5)☒ Claim(s) *8,10-28,30-35,43-52 and 54-81* is/are allowed.

6)☒ Claim(s) *4-7,9,29,36-42,53 and 82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The amendment D filed on 3/3/03 has been entered.

Claims 4-82, 84-108 are pending in the application.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 4-82, drawn to a memory device having a reference cell, classified in class 365, subclass 210.

II. Claims 84-108, drawn to a memory device including a spare (or redundant) array, classified in class 365, subclass 200.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions have different modes of operation. Specifically, the reference cell or circuit in the invention I is used for reading data, and the spare cell or the sprare memory array in the invention II is used for replacing a defective cell in a memory device.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr Edward B Weller on 5/30/03 a provisional election was made without traverse to prosecute the invention of group I, claims 4-82. Affirmation of this election must be made by applicant in replying to this Office action. Claims 84-108 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-7, 9, 29, 36-42 and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4 (second and third paragraphs), the recitation of "one memory decoder" in the second paragraph and the "at least one memory decoder" in the beginning of the third paragraph make the scope of this claim unclear and indefinite. Are these two "one memory decoder" the same, or different memory decoder.

Claims 5-7, 9, 29, 36-42 and 53 are rejected because of their dependency on the rejected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 4-5, 7, 9, 29, 36-39, 53 and 82 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsen U.S. Patent 5,936,906.

For the purpose of this rejection, the memory cells that connected to bit lines BL1 and BL2 and WL—WL4 (figure 4) would be considered as a segmented memory array, and the memory cells that connected to BL3 and BL4 and WL1-WL4 would be considered as another segmented memory array.

Regarding claims 4 and 82, Tsen disclose a data storage system comprising a plurality of multidimensional segmented memory array, each of memory array including a plurality of memory cells (M1-M8, figure 3), a plurality of bit lines (BL1-BL2), a plurality of control gates lines (WL1, WL2, WL3, figure 3) and at least one common line (the line that connects the source line of memory cells in each segment as set forth above), at

least one memory decoder (105 and 142, figure 5) coupled to the memory array for providing bias signal (the output signal of 142, figure 5) to the selected one of the plurality of memory cells, and a reference array (110, figure 2) coupled to the memory array 100 (figure 2) and configurable to provide reference signals used for programming and reading the selected one of the plurality of memory cells (see elements106, 120 and 130 in figure 2, such elements would perform the function of programming and reading data to and from the memory cells).

Regarding claim 5, the reference array 110 (figure 2) clearly comprises a plurality of reference memory cells and both the memory cells and the reference memory cells are biased with approximately similar bias conditions on their control gated, bit lines and common lines.

Regarding claim 7, the bit line decoder 104 (figures 2 and 5) would be a first address decoder.

Regarding claim 9, the word line decoder 102 (figures 2 and 5) would be a third address decoder because this decoder selects one or more control gate lines (WL1-WL4).

Regarding claim 29, the reference cells array 110 in figure 2 clearly operative to provide one reference signal (the signal that applied to 120 in figure 2).

Regarding claims 36 and 37, since the voltage applied to the control gate lines of both memory cells and reference memory cells is a step voltage as shown in figure 6A, the reference signals in reference cells would be 2N and 2N-1 unique levels.

Regarding claims 38 and 39, the reference cells 110 is clearly programmed with a set of reference values and is just one time programming. See column 4, line 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsen in view of Banks (U.S. Patent No 6,002,614)

Tsen applied as above. The difference between Tsen and claims 40-42 is that Tsen fail to disclose a memory device that includes a driver circuit, which has a latch connected to the bit lines for the purpose of latching data in the bit lines.

Banks teaches that the use of a driver having a latch connected to the bit lines so as to latch data in the memory device operation is well known in the memory art. It is noted that the sense amplifier in both Tsen and Banks would perform the function of comparing data on the bit lines and data in the reference cells in the reading modes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tsen by connecting a latch at the input on the bit lines for latching data inputting to the bit lines for the purpose of improving the operation of the memory device as taught by Banks.

Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsen in view of Paterson et al (U.S. Patent No 4,924,437).

Tsen applied as above. Tsen differs from claim 53 by the recitation of an application of 0V to the memory cells that are not selected in a programming mode.

Paterson et al teaches that the application of 0v to the unselected memory cells (unselected bit lines) in a non-volatile memory device in a programming mode (see column 5, line 23-35) is well known in the memory art. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tsen by applying 0V to the memory cells in a programming mode in order to save power as taught by Paterson et al.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsen in view of Kobayashi (U.S. Patent No 5,818,759).

Tsen applied as above. The only difference between Tsen and claim 6 is that Tsen fail to teach the regular cell and the reference cell share a common source line. Note that the regular cell and the reference cell in Tsen share control gate lines or word lines.

Kobayashi (figure 12) discloses a memory device having a memory cell array (122) and a reference cell (300a, 300b), wherein the regular memory cell and the reference cell 300a share the same common line (SL that is connected to 132). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tsen by connecting the source lines of the regular cell and the reference cell together so as to reduce the size of the memory cell and improve the access timing of the memory operation as evidenced by Kaboyashi.

Allowable Subject Matter

Claims 8, 10-28, 30-35, 43-52, 54-81 are allowed.

Response to Arguments

The applicant argues that the reference of Tsen fail to teach a multidimensional segmented memory arrays as shown in figure 2A and 2B. Note that figure 2A and 3A only show a plurality of segmented of multilevel flash memory array, and such feature as clear shown in figure 4 of Tsen. It is noted that two column of memory cells would be considered as a segment, therefore the block of memory cell 110 in figure 4 of Tsen contains a plurality of segments of multilevel flash memory cells.

In response to applicant argument on the reference of Banks, it is noted that any two column of cells in Bank could be an array and the cell in Bank is clearly a multilevel flash memory array i.e. multidimensional memory array.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son t Dinh whose telephone number is 703-308-4120. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 703-308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

S. Dinh
May 31, 2003

Son T. Dinh
Primary Examiner